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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/075,122	02/12/2002	Richard T. Behrens	SILA:078	7298

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O'KEEFE, EGAN & PETERMAN, L.L.P.
Suite 200, Building C
1101 Capital of Texas Highway South
Austin, TX 78746

EXAMINER	
APPIAH, CHARLES NANA	

ART UNIT	PAPER NUMBER
2686	

DATE MAILED: 09/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/075,122	BEHRENS ET AL.	
	Examiner	Art Unit	
	Charles Appiah	2686	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-78* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-33* is/are allowed.

6)☒ Claim(s) *34,61 and 70* is/are rejected.

7)☐ Claim(s) *35-60,62-69 and 71-78* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8,9*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on 12/02.2002 and 09/02/2003 are in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement are being considered by the examiner.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claim 34 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jakobsson (6,757,340).

Regarding claim 34, Jakobsson discloses (with reference to Fig. 2), a radio-frequency (RF) circuitry, comprising: a receiver analog circuitry configured to receive and process a RF input signal (signal from antenna 202 to amplifier 206), to generate a processed RF signal (output of amplifier 232), the receiver analog circuitry including an analog-to-digital converter circuitry (234), adapted to convert the processed RF into a one-bit digital in-phase signal (digital base band I signal 236) and a one-bit digital quadrature signal (digital base band Q signal 238), and a receiver digital circuitry (output of A/D 234), configured to receive the one-bit digital in-phase signal and the one-bit digital quadrature signal, the receiver digital circuitry further configured to process the one-bit digital in-phase signal and the one-bit signal to generate a base band signal (desired signal 254 as output from demodulator 252). Jakobsson thus meet all limitations of claim 34 except the feature of the receiver analog circuitry and receiver digital circuitry being embodied on a first and second integrated circuitry respectively. However, since it has been held that constructing a formerly integral structure in various elements involves routine skill in the art, (see *Nerwin v. Erlichman, 168 USPQ 177, 179)*, it would have been obvious to one of ordinary skill in the art to have Jakobsson's analog circuitry and digital circuitry on different chips (integrated circuits) in order to distribute processing loads as well as reduce interference between the analog and digital circuits.

5. Claim 61 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sointula (6,091,780) in view of Johnson (5,420,592).

Regarding claim 61, Sointula discloses a method of receiving a radio-frequency (RF) signal, comprising: receiving and processing the RF signal within a first circuit that includes receiver analog circuitry configured to generate an analog processed RF signal (output 805 from downconvertor 801 and IQ downconvertor 803), converting the analog processed signal with the first circuit to a digital signal (signal 805 into AD 806 and outputting signal 807), supplying the digital signal via digital interface and receiving the digital signal within a second circuit (signal 807 into IQ downconvertor 808) that includes receiver digital circuitry (DSP 602), mixing the within the digital receiver circuitry the digital signal with a digital IF local oscillator (809) to generate a digital down-converted signal (output of IQ downconvertor 808 into demodulator 810, and processing the digital down converted signal within the receiver digital circuitry to generate a baseband signal (output of data reconstruction circuit 811). Sointula shows in Fig. 8, the analog circuitry (605) and DSP (602) embodying the digital circuitry as separate circuits but fails to specifically disclose the receiver analog circuitry and receiver digital circuitry being embodied on a first and second integrated circuits respectively.

However, since it has been held that constructing a formerly integral structure in various elements involves routine skill in the art, (see *Nerwin v. Erlichman, 168 USPQ 177, 179)*, it would have been obvious to one of ordinary skill in the art to have Sointula's analog circuitry and digital circuitry on different chips (integrated circuits) in order to distribute processing loads as well as reduce interference between the analog and digital circuits.

Sointula as modified fails to explicitly teach the use of a one-bit digital interface for supplying the digital signal. The use of one-bit analog-to-digital converters for supplying digital signals is very well known in the art as taught for example by Johnson. Johnson teaches the use of a one-bit analog-to-digital converter in a remote mobile position processing system in which the one-bit A/D converter ensures low manufacturing costs and maintains a high level of performance (see col. 3, lines 27-36).

It would therefore has been obvious to one of ordinary skill in the art to constitute the A/D circuit of Sointula, as modified as a one-bit A/D in order to provide the desired digital signals with low manufacturing costs while maintaining high performance as taught by Johnson.

6. Claim 70 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zangi (5,999,573) in view of Johnson (5,420,592).

Regarding claim 70, Zangi discloses a method of receiving a RF signal, comprising: (see Fig.1), receiving and processing the RF signal within a first circuit that includes receiver analog circuitry configured to generate an analog processed RF signal (signal being inputted to ADC 20) converting the analog processed RF signal within the first circuit to a digital signal, supplying the digital signal via a digital interface and receiving the digital digital signal within a circuit that includes receiver digital circuitry (feature of ADC 20 outputting signal to digital channelizer 25, see col. 2, lines 19-23), performing digital channelization filtering of the digital signal within the receiver digital circuitry to generate a filtered digital signal (see col. 27-65), and processing the filtered digital signal within the receiver digital circuitry to generate a baseband signal (see col.

4, lines 20-30). Zangi fails to specifically disclose the receiver analog circuitry and receiver digital circuitry being embodied on a first and a second integrated circuitry respectively.

However, since it has been held that constructing a formerly integral structure in various elements involves routine skill in the art, (see *Nerwin v. Erlichman, 168 USPQ 177, 179)*, it would have been obvious to one of ordinary skill in the art to have Zangi's analog circuitry and digital circuitry on different chips (integrated circuits) in order to distribute processing loads as well as reduce interference between the analog and digital circuits.

Zangi as modified fails to explicitly teach supplying digital signal via a one-bit digital interface.

The use of one-bit analog-to-digital converters for supplying digital signals is very well known in the art as taught for example by Johnson. Johnson teaches the use of a one-bit analog-to-digital converter in a remote mobile position processing system in which the one-bit A/D converter ensures low manufacturing costs and maintains a high level of performance (see col. 3, lines 27-36).

It would therefore has been obvious to one of ordinary skill in the art to constitute the A/D circuit of Zangi as modified as a one-bit A/D in order to provide the desired digital signals with low manufacturing costs while maintaining high performance as taught by Johnson.

Allowable Subject Matter

7. Claims 1-33 are allowed.

8. Claims 35-60, 62-69 and 71-78 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The following is a statement of reasons for the indication of allowable subject matter:

With respect to claims 1 and 16, the prior art of record such as Marshall et al. ("A 2.7 V GSM Transceiver ICs with On-chip Filtering), Chung-Hwan et al. ("A 3.3 V Front-end Receiver GaAs MMIC For digital/Analog Dual-mode Hand-held Phones"), Sointula (6,091,780) and Zangi (5,999,573) discloses several digital receiver circuits in different configurations the prior art of record fails to teach or fairly suggest alone or in combination, the receiver digital circuitry including all the limitations as specifically set forth in claims 1 and 16.

With respect to claim 35, the prior art of record such as Zangi discloses a channelizer for processing a received wideband signal. Jakobsson (6,757,340) discloses a radio receiver having an analog circuitry and a digital circuitry. Neither Jakobsson nor any of the prior art of record teach or fairly suggest wherein the receiver digital circuitry further comprises digital down-converter circuitry configured to mix the one-bit digital one-phase signal and the one-bit digital quadrature signal to generate a digital down-converted in-phase and a digital down-converted quadrature signal in combination with the recited limitations of claim 35.

With respect to claim 62, Sointula discloses a method of receiving a RF signal that includes : receiving and processing the RF signal within a first circuit that includes

receiver analog circuitry configured to generate an analog processed RF signal, converting the analog processed signal with the first circuit to a digital, supplying the digital signal via digital interface and receiving the digital signal within a second circuit that includes receiver digital circuitry, mixing the digital within the digital receiver circuitry the digital signal with a digital IF local oscillator to generate a digital down-converted signal, and processing the digital down converted signal within the receiver digital circuitry to generate a baseband. Sointula fails to teach or fairly suggest alone or in combination, the feature of processing the digital down-converted signal further comprises performing digital channelization filtering of the down-converted signal to generate a filtered digital signal in combination with all the recited features of claim 62.

With respect to claim 71, Zangi discloses a method of receiving a RF signal, comprising: (see Fig.1), receiving and processing the RF signal within a first circuit that includes receiver analog circuitry configured to generate an analog processed RF signal converting the analog processed RF signal within the first circuit to a digital signal, supplying the digital signal via a digital interface and receiving the digital I signal within a circuit that includes receiver digital circuitry, performing digital channelization filtering of the digital signal within the receiver digital circuitry to generate a filtered digital signal and processing the filtered digital signal within the receiver digital circuitry to generate a baseband signal. Zangi fails to teach or fairly suggest, alone or in combination the feature of processing the filtered signal further comprises mixing the filtered digital signal with digital intermediate frequency local oscillator signal to generate a digital down-converted signal in combination with all the other limitations of claim 71.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Terlep et al. (5,796,777) discloses an apparatus for digitizing and detecting a received radio frequency signal.

Murphy et al. (5,955,987) discloses a hybrid RF system having analog and digital sections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Charles Appiah whose telephone number is 703 305-4772. The examiner can normally be reached on M-F 7:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marsha Banks-Harold can be reached on 703 305-4379. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CA
24 September 2004

CHARLES APPIAH
PRIMARY EXAMINER